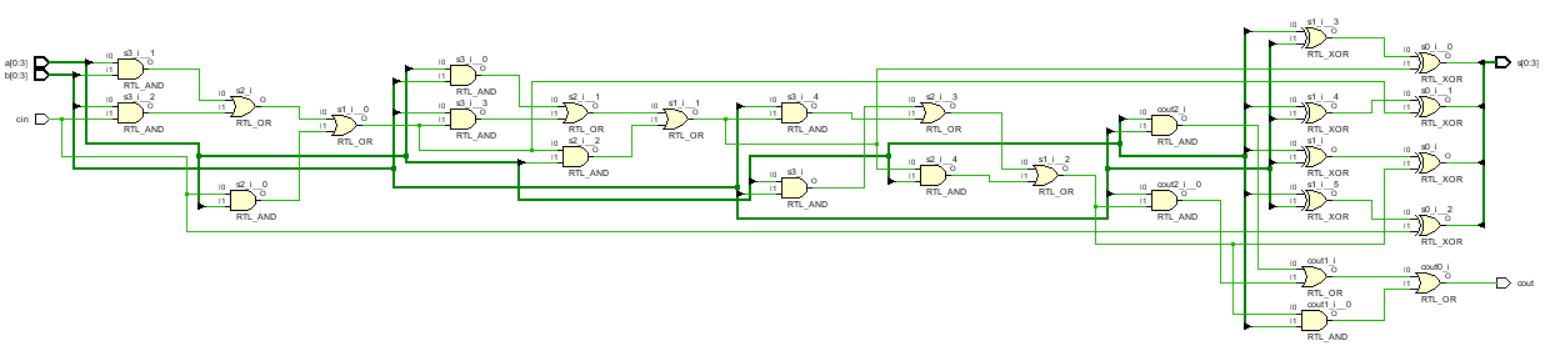
**Practical 4**

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| --- | --- | --- |
| |  |  | | --- | --- | | |  | | --- | | **Aim:**Write a VHDL code for 4 bit ripple carry adder using loop statement. | |   **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  entity ripplecarryadder\_4bit is  Port ( a : in STD\_LOGIC\_VECTOR (0 to 3);  b : in STD\_LOGIC\_VECTOR (0 to 3);  cin : in STD\_LOGIC;  s : out STD\_LOGIC\_VECTOR (0 to 3);  cout : out STD\_LOGIC);  end ripplecarryadder\_4bit;  architecture Behavioral of ripplecarryadder\_4bit is  begin  process(a,b,cin)  variable i:INTEGER:=0;  variable c:std\_logic\_vector(0 to 4):="00000";  begin  c(0):=cin;    lop: for i in 0 to 3 loop    s(i)<=a(i) xor b(i) xor c(i);  c(i+1):=(a(i) and b(i)) or (b(i) and c(i)) or (c(i) and a(i));    end loop lop;  cout <= c(4);  end process;    end Behavioral; |

**RTL DIAGRAM:**

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**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_ripplecarryadder\_4bit is

-- Port ( );

end Tb\_ripplecarryadder\_4bit;

architecture Behavioral of Tb\_ripplecarryadder\_4bit is

component ripplecarryadder\_4bit is

Port ( a : in STD\_LOGIC\_VECTOR (0 to 3);

b : in STD\_LOGIC\_VECTOR (0 to 3);

cin : in STD\_LOGIC;

s : out STD\_LOGIC\_VECTOR (0 to 3);

cout : out STD\_LOGIC);

end component ripplecarryadder\_4bit;

signal a : STD\_LOGIC\_VECTOR (0 to 3);

signal b : STD\_LOGIC\_VECTOR (0 to 3);

signal cin :STD\_LOGIC;

signal s : STD\_LOGIC\_VECTOR (0 to 3);

signal cout :STD\_LOGIC;

begin

u1:ripplecarryadder\_4bit port map(a,b,cin,s,cout);

process

begin

cin<='0';

a<="0000";

b<="0000";

wait for 10ns;

b<="0001";

wait for 10ns;

b<="0010";

wait for 10ns;

b<="0011";

wait for 10ns;

b<="0100";

wait for 10ns;

b<="0101";

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wait for 10ns;

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wait for 10ns;

b<="0111";

wait for 10ns;

b<="1000";

wait for 10ns;

b<="1001";

wait for 10ns;

b<="1010";

wait for 10ns;

b<="1011";

wait for 10ns;

b<="1100";

wait for 10ns;

b<="1101";

wait for 10ns;

b<="1110";

wait for 10ns;

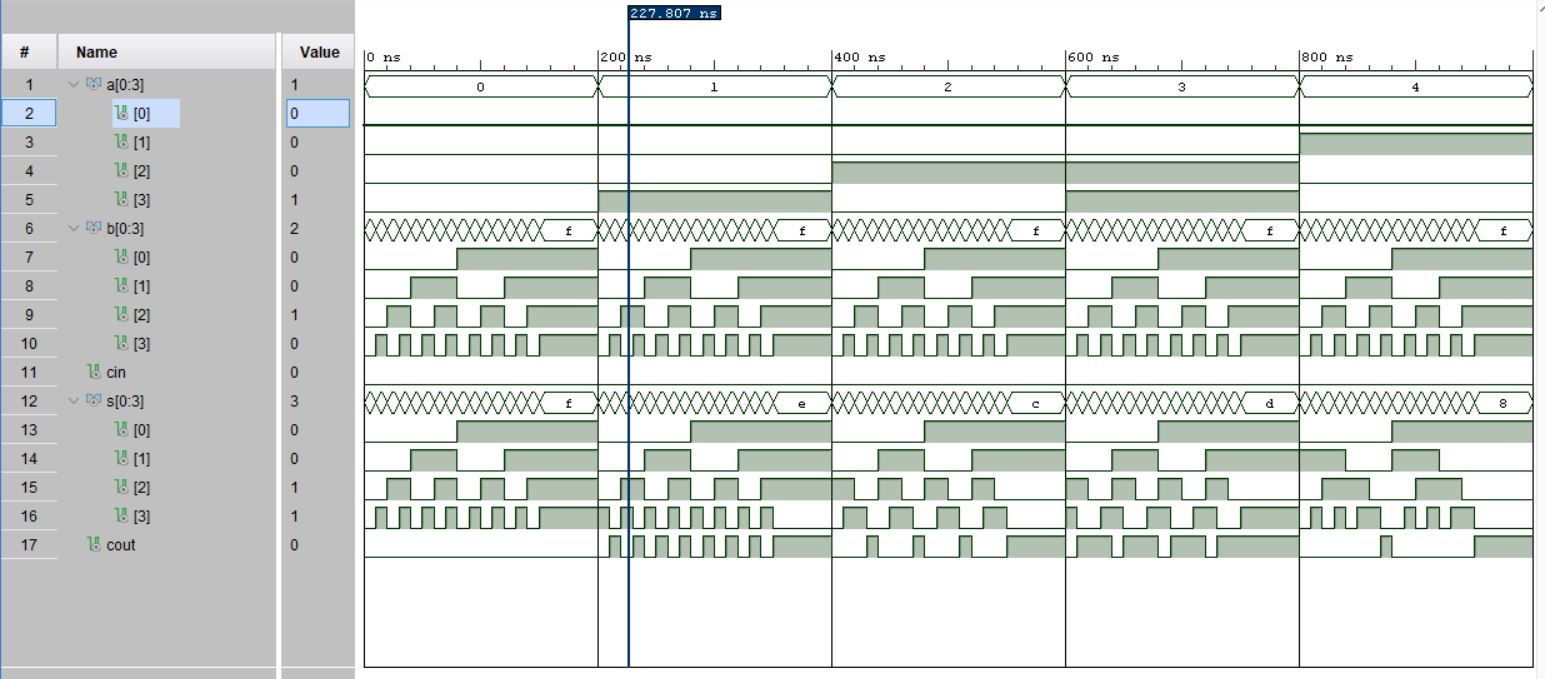
b<="1111";

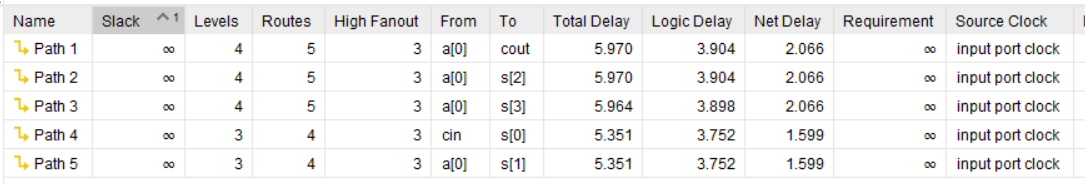
wait for 50ns;

end process;

end Behavioral;

**SIMULATION WAVEFORM :**

****



**SYNTHESIS SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Resource** | **Utilization** | **Available** | **Utilization %** |
| LUT | 4 | 17600 | 0.02 |
| IO | 14 | 100 | 14.00 |

Maximum Combinational Delay: 5.970nSec